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Title: METHOD AND APPARATUS FOR TESTING A MEMORY DEVICE WITH COMPRESSED DATA USING A SINGLE OUTPUT

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UNITED STATES PATENT APPLICATION

METHOD AND APPARATUS FOR TESTING A MEMORY DEVICE WITH COMPRESSED DATA USING A SINGLE OUTPUT

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METHOD AND APPARATUS FOR TESTING A MEMORY DEVICE WITH COMPRESSED DATA USING A SINGLE OUTPUT

Field of the Invention

The present invention relates to memory devices, and more particularly, to a method and apparatus for testing a memory device with compressed data using a single output.

Background

An integrated circuit comprises a large number of semiconductor devices, such as transistors and capacitors, that are fabricated in a dense pattern on a semiconductor substrate. Groups of integrated circuits are fabricated on a single wafer of semiconductor material, and a very large number of devices are fabricated on each wafer. Typically many of the devices on a wafer contain defects which render a portion of the integrated circuits unsalable, so each integrated circuit must be tested before being shipped to a customer.

Different types of integrated circuits are tested in different ways. Integrated circuit memory devices are tested in groups, for example four or more at a time, by a single automatic test machine. The memory devices contain arrays of memory cells arranged in rows and columns The test machine writes data to the cells in a pattern and then reads the data from the cells. If a the data read from a cell is different from the data that was written to it, the cell is defective. Most memory devices contain redundant cells that are used to replace cells discovered to be defective in such a test.

The process of writing data to and reading data from each cell in a memory device is extremely time consuming and a costly part of the fabrication process. Most methods of testing memory devices read data from a large number of cells and then compress the

read data before evaluating the results of the test. The data is compressed in a dedicated test circuit in the memory device that is used only during the test. In a typical test sequence all 1's or all 0's are written to a pattern of cells in the memory device and if all of the tested cells are operating properly the read data will be all 1's or all 0's. However, if one or more of the cells malfunctions the read data will have both 1's and 0's. The test circuit will output a 1 to a selected data pin if the read data is all 1's, and will output a 0 to the data pin if the read data is all 0's. If the read data contains 0's and 1's the data pin is tri-stated by the test circuit. Waiting for the tri-state output to settle, or in other words waiting for the data pin to reach a high-impedance state, adds a significant amount of time to the test process. Even with the use of compressed data a test of a single memory device is time consuming and costly.

There is a need for faster methods of testing integrated circuit memory devices to reduce the cost of fabricating such devices.

Summary of the Invention

The above mentioned and other deficiencies are addressed in the following detailed description of embodiments of the present invention. According to one embodiment of the present invention data is written to cells in a memory device, the cells are read to generate read data, the read data is compressed to generate test data, and the test data is produced at a single output on edges of a clock signal. Advantages of the present invention will be apparent to one skilled in the art upon an examination of the detailed description of the embodiments of the present invention.

Brief Description of the Drawings

Figure 1 is a block diagram of a memory system according to an embodiment of the present invention.

Figure 2 is a block diagram of a test circuit according to an embodiment of the present invention.

Figure 3 is an electrical schematic diagram of a latch circuit shown in the test circuit of Figure 2 according to an embodiment of the present invention.

Figure 4 is an electrical schematic diagram of a logic circuit shown in the test circuit of Figure 2 according to an embodiment of the present invention.

Figure 5 is a flow chart of a method for testing a memory device according to an embodiment of the present invention.

Figure 6 is a block diagram of a system for implementing the method shown in Figure 5 according to an embodiment of the present invention.

Figure 7 is a block diagram of a system for testing memory devices according to an embodiment of the present invention.

Figure 8 is a block diagram of an information handling system according to an embodiment of the present invention.

Detailed Description of the Preferred Embodiments

In the following detailed description of exemplary embodiments of the present invention, reference is made to the accompanying drawings which form a part hereof, and in which are shown by way of illustration specific exemplary embodiments in which the present invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical, electrical and other changes may be made without departing from the spirit or scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

In this description transistors will be described as being in an active state or switched on when they are rendered conductive by an appropriate control signal, and the transistors will be described as being in an inactive state or switched off when they are rendered non-conductive by the control signal.

Memory devices are tested and operated in conjunction with an electronic control circuit. Figure 1 is a block diagram a memory system 100 according to an embodiment of the present invention. The memory system 100 includes a memory device 102 having an array 114 of memory cells. An addressing circuit 116 is coupled to the array 114 to select cells for reading or writing data. The array 114 receives data from and provides data to a set of data lines 118. Addresses are provided to the addressing circuit 116 over a set of address lines 120, and control signals are provided to the addressing circuit 116 over a set of control lines 122 to control the operation of the memory device 102. The memory device 102 is coupled to an electronic control circuit 124 through the data lines 118, the address lines 120, and the control lines 122. The control circuit 124 may be a processor or a test control circuit coupled to test the memory device 102. The data, address, and control lines 118, 120, 122 form a bus outside the memory device 102, and the bus is connected to the memory device 102 through a set of external pins. The control circuit 124 governs a test of the memory device 102 by providing write data, addresses, and control signals over the data, address, and control lines 118, 120, 122, respectively, to the memory device 102. During the test the memory device 102 returns read data to the control circuit 124 over the data lines 118.

The memory device 102 is tested by writing a single test data value to a plurality of selected cells in the array 114. Those skilled in the art will understand that this is typically done by converting one bit into a plurality of bits through a dedicated circuit and writing the bits to the selected cells. Data is then read from the selected cells to determine if the read data is the same as the test data value. A single test data value, either a 1 or a 0, is used to speed the test by enabling a rapid analysis of the read data. If the memory device 102 is operating properly the read data will be either all 1's or all 0's.

In one embodiment of the present invention the array 114 is divided into as many as 256 subarrays of cells. The test data value is written to a selected cell in each of 16 of the subarrays so that the change in each selected cell does not interfere with the writing to other selected cells. The selected cells are then read to generate 16 read data values. The

read data values are compressed to generate one or more compressed data signals that are analyzed to determine if the read data values are the same as the test data value. The compression of the read data values reduces the time necessary to test the memory device 102 because the read data values do not have to be analyzed individually. Dedicated test circuitry is provided in either the memory device 102 or the control circuit 124 to carry out the compression of the read data values. The test is repeated for different groups of selected cells until all of the cells in the array 114 have been tested. In alternative embodiments of the present invention the test is repeated for different groups of cells until both a 0 and a 1 have been written to and read from all of the cells in the array 114. This may be accomplished by writing 0's and 1's to the cells in a checkerboard pattern, or by using other patterns known to those skilled in the art.

A test circuit 200 according to an embodiment of the present invention is shown in Figure 2. The test circuit 200 compresses the read data values from the memory device 102 provided on sixteen read data paths 202 during the test. Each of the read data paths 202 includes a respective latch circuit 204 that holds the read data value for a short period of time. The read data paths 202 and the latch circuits 204 are used during a non-test operation of the memory device 102 to transfer data from the cells in the array 114 to respective output pins. Two intermediate signals PAR0 and PAR1 are generated in a circuit connecting the latch circuits 204 based on the read data values. The signals PAR0 and PAR1 are coupled to a logic circuit 206 in which they are manipulated to generate two compressed data signals DRT and DRTi provided at two outputs of the logic circuit 206. The logic circuit 206 is structured to generate the signals DRT and DRTi to be equal to the read data values if the read data values are all the same, and to be different from each other if the read data values include both 0's and 1's. The signals DRT and DRTi are provided to a double data rate (DDR) circuit 208 that combines the signals DRT and DRTi into a single test output signal at a pin 210. The DDR circuit 208 receives a clock signal from a clock signal source 212 and alternately couples the signals DRT and DRTi to the pin 210 on successive edges of the clock signal. For example, in a single period of

the clock signal the signal DRT is coupled to the pin 210 on the rising edge and the signal DRTi is coupled to the pin 210 on the falling edge of the clock signal.

The test output signal is strobed by the control circuit 124 with either an edge strobe or a window strobe. If the test data value is 0 and all the read data values are 0 then the signals DRT and DRTi are both 0, the test output signal is low, and the selected cells have successfully stored and produced the test data value. If the test data value is 1 and all the read data values are 1 then the signals DRT and DRTi are both 1, the test output signal is high, and the selected cells have successfully stored and produced the test data value. However, if the read data values are 0's and 1's then the signals DRT and DRTi are different, the test output signal toggles between high and low over one period of the clock signal, and some of the selected cells have failed to store the test data properly. The control circuit 124 then replaces the failed cells according to methods known to those skilled in the art.

The test circuit 200 is coupled to the read data paths 202 in the array 114 and may be located in the array 114, somewhere else in the memory device 102, or in the control circuit 124.

Several implementations of the DDR circuit 208 are known to those skilled in the art. At least two different types of a DDR synchronous dynamic random-access memory (SDRAM) and a synchronous graphics random-access memory (SGRAM) have been proposed. A first standard for DDR SDRAM/SGRAM has been implemented by Samsung Electronics Co., of Suwon, South Korea, in its KM432D5131 DDR SGRAM, a data sheet for which, Revision 0.6 (April 1998) has been published. A second standard has been agreed to by the members of the Joint Electronic Device Engineering Council (JEDEC). An example of a DDR SDRAM/SGRAM according to this latter standard is the IBM DDR SGRAM IBM0616328RL6A, manufactured by International Business Machines (IBM), Inc., of White Plains, N.Y., a data sheet for which, #06L6370-02 (12/97), has been published.

A detailed electrical schematic diagram of one of the latch circuits 204 is shown in Figure 3, and a detailed electrical schematic diagram of the logic circuit 206 is shown in Figure 4 according to an embodiment of the present invention. The structure and operation of these circuits will be described together. Elements shown in Figure 2 retain the reference characters shown in Figure 2.

The latch circuit 204 is part of the read data path 202 on which is provided a read data value from a cell in the array 114. The read data value is latched by a pair of inverters 310. The latch circuit 204 is used when the memory device 102 is operating in a non-test mode to output the read data value to a pin 320. The inverters 310 are connected to a set of N-channel pull-down transistors 330, 332, 334 that compress the read data values latched in the sixteen latch circuits 204 shown in Figure 2 into the signals PAR0 and PAR1. A control signal is also provided to the latch circuit 204. The operation of the pull down transistors 330, 332, 334 will be explained with reference to the logic circuit 206.

Two control signals DCF0 and DCF1 are provided to the logic circuit 206 to control the compression of the read data values. The signals DCF0 and DCF1 are normally low such that two P-channel pull-up transistors 410 are switched on to raise the voltage of lines carrying the signals PAR0 and PAR1. The signals DCF0 and DCF1 are used to generate two more control signals F0 and F1 through a set of inverters, and the signals F0 and F1 are coupled to control terminals of a number of pull-down transistors including the pull-down transistor 330 in the latch circuit 204.

The logic circuit 206 generates the signals DRT and DRTi in the following manner. When the signals DCF0 and DCF1 are low the lines carrying the signals PAR0 and PAR1 are high and a read data value is latched by the inverters 310. Next, the signals DCF0 and DCF1 are brought high to switch off the transistors 410 and the signals F0 and F1 switch on the transistor 330. The read data value latched by the inverters 310 causes one of the transistors 332, 334 to be switched on and the other to be switched off such that PAR0 and PAR1 have different values. The transistor 332, 334 that is switched on is

coupled to ground through the transistor 330 to discharge its respective line. Meanwhile a clock signal DCLAT in the logic circuit 206 causes two flip flop circuits 412 to latch the signals PAR0 and PAR1 before the signals DCF0 and DCF1 are returned to low. Additional logic circuitry shown in Figure 4 generates the signals DRT and DRTi from the signals PAR0 and PAR1 latched in the flip-flop circuits 412 in a manner known to those skilled in the art.

As shown in Figure 2, the latch circuits 204 and the logic circuit 206 operate to compress read data values from up to 16 read data paths 202, and the generation of the signals DRT and DRTi will now be explained in more detail. When the read data values held by the inverters 310 in the latch circuits 204 are all the same, for example 0 or 1, only one of the transistors 332, 334 will be switched on to bring one of the signals PAR0, PAR1 low while the other remains high when the transistor 330 is switched on. The logic circuit 206 subsequently generates the signals DRT and DRTi to be both 1 if all the read data values are 1 and to be both 0 if all the read data values are 0. However, if the read data values are not all the same then both of the transistors 332, 334 will be switched on to bring both signals PAR0, PAR1 low. This due to the fact that each read data value is inverted by the inverters 310 and a 1 is applied to the control terminal of each of the transistors 332, 334 by at least one of the latch circuits 204. When both PAR0 and PAR1 are low the logic circuit 206 generates the signal DRT to be low and the signal DRTi to be high. The signals DRT and DRTi are then combined in the DDR circuit 208 and analyzed as described above with reference to Figure 2.

The signals DCF0 and DCF1 may be manipulated to limit the above-described procedure to 8 read data values for 8 cells instead of the 16 read data values described above. If 8 cells are tested at a time instead of 16 and one is found defective then fewer cells need to be replaced with redundant cells. However, a test of 8 cells at a time is slower than a test of 16 cells at a time.

A flowchart of a method 500 for testing the memory device 102 according to an embodiment of the present invention is shown in Figure 5. A test data value is written to

selected cells in the memory device 102 in step 510 and the selected cells are read in step 512 to generate read data. In step 514 the read data is analyzed and if all the read data is the same then two compressed data signals are generated in step 516 to be equal to the read data. However, if the read data is not all the same then two compressed data signals are generated in step 518 having different values. In step 520 the two compressed data signals, generated either in step 516 or step 518, are output sequentially at a single output as a DDR signal.

The method 500 may be implemented as a series of programmable instructions stored and executed in the control circuit 124. The method 500 may also be implemented in hardware by a system 600 shown in Figure 6. The system 600 includes an electronic control circuit 610, a memory device 612, a bus 614, a write circuit 616, and a read and data compression circuit 618. The system 600 may include one or more of the following: hardwired logic, a Field Programmable Gate Array (FPGA), a hardwired FPGA, programmable logic, a programmable microcontroller, an Application Specific Integrated Circuit (ASIC), a Read Only Memory (ROM) , or a sequencer, or any suitable combination thereof.

A system 700 for testing memory devices according to an embodiment of the present invention is shown in Figure 7. The system 700 includes a test machine 710 and four memory devices 720 each coupled to the test machine 710 to be tested at the same time. The circuitry shown in Figures 2-4 may be located in the test machine 710 or in each of the memory devices 720. In an alternative embodiment of the present invention the method 500 may be implemented as a series of programmable instructions stored and implemented in the test machine 710.

Figure 8 is a block diagram of an information handling system 800 according to another embodiment of the present invention. The system 800 includes a processor 810, a display unit 820, an input/output (I/O) device 830, and a memory device 840. The processor 810, the display unit 820, the input/output (I/O) device 830, and the memory device 840 are coupled together by a suitable communication line or bus 850. The

memory device 840 may include any of the embodiments of the present invention described above which one skilled in the art will appreciate may be employed with any type of memory device having an array of memory cells. Examples of such memory devices include a random-access memory (RAM) such as a dynamic random-access memory (DRAM), a SDRAM, a SGRAM, a static random-access memory (SRAM), or a read-only memory (ROM). The I/O device 830 may be a pointing device such as a mouse, a keyboard, a modem, or any other type of device that transfers data to and from a processor-based system. The display unit 820 may be a monitor. In various embodiments, the information-handling system 800 is a computer system (such as, for example, a video game, a handheld calculator, a personal computer, or a multiprocessor supercomputer), an information appliance (such as, for example, a cellular telephone, a pager, or a daily planner or organizer), an information component (such as, for example, a magnetic disk drive or telecommunications modem), or other appliance (such as, for example, a hearing aid, washing machine or microwave oven having an electronic controller).

The embodiments of the present invention described above provide for a test of a memory device in a faster manner than is presently known or used. Read data values for a test are compressed into a set of signals that are combined in a DDR circuit to be read together at a single output. The set of signals, output on sequential edges of a clock signal, indicate the three possible results of a test of the memory device without requiring that an output pin be tri-stated to indicate one of the results. Those skilled in the art will understand that a significant amount of time is required to bring an output buffer to the tri-state condition, and therefore a memory device may be tested much more rapidly according to the embodiments of the invention. All components of the embodiments of the invention described above may be in the memory device, or some or all of the components may be external to the memory device.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is

calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of the present invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.

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WHAT IS CLAIMED IS:

1. A circuit comprising:

a compression circuit coupled to receive data values and being structured to generate compressed data based on the data values; and

an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

2. The circuit of claim 1 wherein:

the compression circuit is coupled to receive the data values from a plurality of cells in a memory device and is structured to generate first and second compressed data signals based on the data values, the first and second compressed data signals being equal to the data values if the data values are all the same and the first and second compressed data signals being different if the data values are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second compressed data signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first compressed data signal during a leading edge of the clock signal and to produce the second compressed data signal during a trailing edge of the clock signal within each cycle of the clock signal.

3. The circuit of claim 2 wherein the compression circuit comprises:

a plurality of pull-up transistors coupled to intermediate nodes and structured to bring the intermediate nodes to a high voltage;

a plurality of pull-down transistors coupled between data latches structured to latch the data values and the intermediate nodes, the pull-down transistors being structured to generate intermediate signals at the intermediate nodes based on the data values; and

a logic circuit coupled between the intermediate nodes and the double data rate circuit, the logic circuit being structured to generate the first and second compressed data signals based on the intermediate signals.

4. A circuit comprising:

a compression circuit having a plurality of inputs each coupled to receive a data signal and a plurality of compression outputs, the compression outputs being fewer than the inputs, the compression circuit being structured to generate a compressed data signal at each of the compression outputs based on the data signals; and

an output circuit coupled to the compression circuit and being structured to couple each compressed data signal to a single output on edges of a clock signal.

5. The circuit of claim 4 wherein:

the compression circuit is structured to generate first and second signals at first and second compression outputs based on the data signals, the first and second signals being equal to the data signals if the data signals are all the same and the first and second signals being different if the data signals are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first signal during a leading edge of the clock signal and to produce the second signal during a trailing edge of the clock signal within each cycle of the clock signal.

6. The circuit of claim 5, further comprising:

a plurality of latch circuits, each latch circuit having an input coupled to a read data path to receive a respective one of the data signals from a memory cell in a memory device and having a pair of inverters each having an output connected to an input of the

other inverter to hold the data signal, the latch circuits being coupled together to the compression circuit; and

the inputs of the compression circuit are coupled to the latch circuits to receive the data signals.

7. The circuit of claim 6 wherein the compression circuit comprises:

a plurality of pull-up transistors coupled to intermediate nodes and structured to bring the intermediate nodes to a high voltage;

a plurality of pull-down transistors coupled between the latch circuits and the intermediate nodes, the pull-down transistors being structured to generate intermediate signals at the intermediate nodes based on the data signals; and

a logic circuit coupled between the intermediate nodes and the double data rate circuit, the logic circuit being structured to generate the first and second signals based on the intermediate signals.

8. A memory device comprising:

a plurality of cells;

a compression circuit coupled to receive data values from the cells and being structured to generate compressed data based on the data values; and

an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

9. The memory device of claim 8 wherein:

the compression circuit is structured to generate first and second compressed data signals based on the data values, the first and second compressed data signals being equal to the data values if the data values are all the same and the first and second compressed data signals being different if the data values are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second compressed data signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first compressed data signal during a leading edge of the clock signal and to produce the second compressed data signal during a trailing edge of the clock signal within each cycle of the clock signal.

10. The memory device of claim 9, further comprising:

addressing circuitry;

control lines;

address lines; and

data lines.

11. The memory device of claim 10 wherein the compression circuit comprises:

a plurality of data latches, each data latch having an input coupled to a read data path to receive a data value read from one of the cells and a pair of inverters coupled to receive the data value, each inverter having an output connected to an input of the other inverter to hold the data value;

a plurality of pull-up transistors coupled to intermediate nodes and structured to bring the intermediate nodes to a high voltage;

a plurality of pull-down transistors coupled between the data latches and the intermediate nodes, the pull-down transistors being structured to generate intermediate signals at the intermediate nodes based on the data values;

a logic circuit coupled between the intermediate nodes and the double data rate circuit, the logic circuit being structured to generate the first and second compressed data signals based on the intermediate signals.

12. A system comprising:

a processor;

a memory device having a plurality of cells; and

a test circuit comprising:

a compression circuit coupled to receive data values from the cells and being structured to generate compressed data based on the data values; and

an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

13. The system of claim 12 wherein:

the compression circuit is structured to generate first and second signals at first and second compression outputs based on the data values, the first and second signals being equal to the data values if the data values are all the same and the first and second signals being different if the data values are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first signal during a leading edge of the clock signal and to produce the second signal during a trailing edge of the clock signal within each cycle of the clock signal.

14. The system of claim 13, further comprising:

an input/output device; and

a bus connected to the processor, the memory device, and the input/output device.

15. The system of claim 13, further comprising:

a test machine including the processor;

a write circuit;

a read and data compression circuit including the test circuit; and

wherein the test machine, the write circuit, the read and data compression circuit, and the memory device are connected together by communication lines.

16. A system comprising:

a processor; and

a memory device having a plurality of cells and being connected to the processor, the memory device having an internal test circuit comprising:

a compression circuit coupled to receive data values from the cells and being structured to generate compressed data based on the data values; and

an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

17. The system of claim 16 wherein:

the compression circuit is structured to generate first and second signals at first and second compression outputs based on the data values, the first and second signals being equal to the data values if the data values are all the same and the first and second signals being different if the data values are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first signal during a leading edge of the clock signal and to produce the second signal during a trailing edge of the clock signal within each cycle of the clock signal.

18. The system of claim 17, further comprising:

a display unit;

an input/output device; and

a bus coupling the processor, the memory device, the display unit, and the input/output device.

19. The system of claim 18 wherein the system comprises a computer system, an information component, or an appliance.

20. A test system comprising:

a test machine;

a memory device having a plurality of cells and being coupled to the test machine to be tested; and

test circuitry comprising:

a compression circuit coupled to receive data signals from the cells and being structured to generate compressed data based on the data signals; and

an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

21. The system of claim 20 wherein:

the compression circuit is structured to generate first and second signals at first and second compression outputs based on the data signals, the first and second signals being equal to the data signals if the data signals are all the same and the first and second signals being different if the data signals are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first signal during a leading edge of the clock signal and to produce the second signal during a trailing edge of the clock signal within each cycle of the clock signal.

22. The system of claim 21, further comprising a plurality of memory devices each having a plurality of cells, each of the memory devices being coupled to the test machine to be tested.

23. The system of claim 21 wherein the test circuitry is located in the memory device.

24. The system of claim 21 wherein the test circuitry is located in the test machine.

25. The system of claim 21 wherein the test circuitry is located between the test machine and the memory device.

26. A double data rate memory device comprising:

a plurality of cells;

a compression circuit coupled to receive data values from the cells and being structured to generate compressed data based on the data values; and

an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

27. The memory device of claim 26 wherein:

the compression circuit is structured to generate first and second compressed data signals based on the data values, the first and second compressed data signals being equal to the data values if the data values are all the same and the first and second compressed data signals being different if the data values are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second compressed data signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first compressed data signal during a leading edge of the clock signal and to produce the second compressed data signal during a trailing edge of the clock signal.

28. The memory device of claim 27, further comprising:

addressing circuitry;

control lines;

address lines;

data lines; and

a plurality of data latches, each data latch having an input coupled to a read data path to receive a data value read from one of the cells and a pair of inverters coupled to receive the data value, each inverter having an output connected to an input of the other inverter to hold the data value, the data latches being coupled together to the compression circuit.

29. The memory device of claim 28 wherein the compression circuit comprises:

a plurality of pull-up transistors coupled to intermediate nodes and structured to bring the intermediate nodes to a high voltage;

a plurality of pull-down transistors coupled between the data latches and the intermediate nodes, the pull-down transistors being structured to generate intermediate signals at the intermediate nodes based on the data values;

a logic circuit coupled between the intermediate nodes and the double data rate circuit, the logic circuit being structured to generate the first and second compressed data signals based on the intermediate signals.

30. A memory device comprising:

a plurality of memory cells;

means for compressing a plurality of data values read from selected ones of the memory cells into test data; and

means for producing the test data on edges of a clock signal.

31. A method for testing a memory device comprising:

writing data to cells in the memory device;

reading the cells to generate read data;

compressing the read data to generate test data; and

producing the test data at a single output on edges of a clock signal.

32. The method of claim 31 wherein:

compressing the read data comprises compressing the read data into two compressed data signals; and

producing the test data comprises alternately coupling the two compressed data signals to the single output on rising and falling edges of the clock signal.

33. The method of claim 32 wherein:

compressing the read data comprises generating first and second compressed data signals to be equal to the read data if all the read data are the same and generating the first and second compressed data signals to be different if all the read data are not the same; and

producing the test data comprises coupling the first and second compressed data signals to a double data rate circuit structured to couple the first compressed data signal to the single output on a rising edge of the clock signal and coupling the second compressed data signal to the single output on a falling edge of the clock signal.

34. The method of claim 33, further comprising analyzing the first and second compressed data signals at the single output to determine that the cells store data properly if the first and second compressed data signals are the same and to determine that the cells do not store data properly if the first and second compressed data signals are not the same.

35. A method for testing a plurality of memory devices comprising:

writing data to cells in each memory device;

reading the cells to generate read data;

compressing the read data from each memory device to generate test data; and

producing the test data for each memory device at a single output on edges of a clock signal.

36. The method of claim 35 wherein:

compressing the read data comprises compressing the read data into two compressed data signals for each memory device; and

producing the test data comprises alternately coupling the two compressed data signals to the single output for each memory device.

37. The method of claim 36 wherein:

compressing the read data comprises, for each memory device, generating first and second compressed data signals to be equal to the read data of the memory device if all the read data from the memory device are the same and generating the first and second compressed data signals to be different if all the read data from the memory device are not the same; and

producing the test data comprises coupling the first and second compressed data signals for each memory device to a double data rate circuit structured to couple the first compressed data signal to the single output on a rising edge of the clock signal and to couple the second compressed data signal to the single output on a falling edge of the clock signal.

38. A method for operating an integrated circuit test machine comprising:

writing a test data value to selected cells in each of a plurality of memory devices;

reading the selected cells to generate read data for each memory device;

compressing the read data for each memory device into test data;

producing the test data for each memory device at a single output on edges of a clock signal; and

analyzing the test data at each output to determine if the selected cells in each memory device have stored the test data value properly.

39. The method of claim 38 wherein:

compressing the read data comprises compressing the read data into two compression signals for each memory device; and

producing the test data comprises alternately coupling the two compression signals to the single output for each memory device.

40. The method of claim 39 wherein:

compressing the read data comprises, for each memory device, generating first and second compression signals to be equal to the read data if all the read data are the same and generating the first and second compression signals to be different if all the read data are not the same; and

producing the test data comprises coupling the first and second compression signals for each memory device to a double data rate circuit structured to couple the first compression signal to the single output on a rising edge of the clock signal and to couple the second compression signal to the single output on a falling edge of the clock signal.

41. The method of claim 40 wherein analyzing the test data comprises analyzing the first and second compression signals at each output to determine that the selected cells stored the test data value properly if the first and second compression signals are the same and to determine that the selected cells did not store the test data value properly if the first and second compression signals are not the same.

42. A method for testing a memory device comprising:

writing data to cells in the memory device;

reading the cells to generate read data;

a step for compressing the read data into test data; and

a step for producing the test data at a single output.

43. A method for testing a memory device comprising:

selecting a plurality of test cells from cells in the memory device;

writing a test data value to each of the selected cells;

reading each selected cell to generate a plurality of read data values;

latching the read data values;

compressing the read data values into two intermediate data values;

converting the intermediate data values into first and second compressed data values, the first and second compressed data values being equal to the read data values if the read data values are all the same, the first and second compressed data values being different if the read data values are not all the same;

generating a clock signal;

producing the first compressed data value at an output on a rising edge in a single period of the clock signal;

producing the second compressed data value at the output on a falling edge in the single period of the clock signal; and

analyzing the first and second compressed data values at the output to determine that the cells in the memory device stored the test data value properly if the first and second compressed data values are equal.

44. A method for testing a double data rate memory device comprising:

writing data to cells in the memory device;

reading the cells to generate read data;

compressing the read data to generate test data; and

producing the test data at an output of a double data rate circuit on edges of a clock signal.

45. The method of claim 44 wherein:

compressing the read data comprises generating first and second compressed data signals to be equal to the read data if all the read data are the same and generating the first and second compressed data signals to be different if all the read data are not the same; and

producing the test data comprises coupling the first compressed data signal to the output of the double data rate circuit on a rising edge of the clock signal and coupling the second compressed data signal to the output of the double data rate circuit on a falling edge of the clock signal.

METHOD AND APPARATUS FOR TESTING A MEMORY DEVICE WITH COMPRESSED DATA USING A SINGLE OUTPUT

ABSTRACT OF THE DISCLOSURE

A method and apparatus for testing a memory device with compressed data using multiple clock edges is disclosed. In one embodiment of the present invention data is written to cells in a memory device, the cells are read to generate read data, the read data is compressed to generate test data, and the test data is produced at a single output on edges of a clock signal.

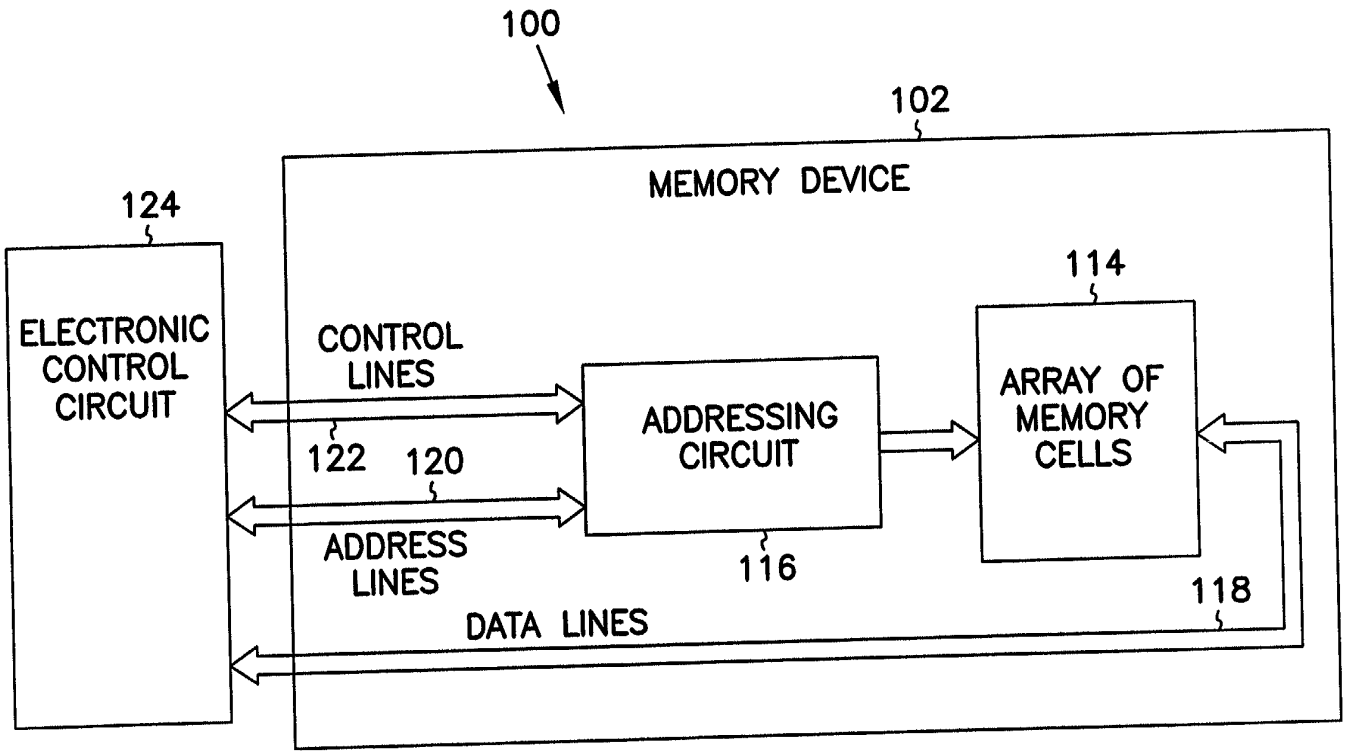
100
102
MEMORY DEVICE
124
ELECTRONIC CONTROL CIRCUIT
CONTROL LINES
122
120
ADDRESS LINES
ADDRESSING CIRCUIT
116
114
ARRAY OF MEMORY CELLS
118
DATA LINES

FIG. 1

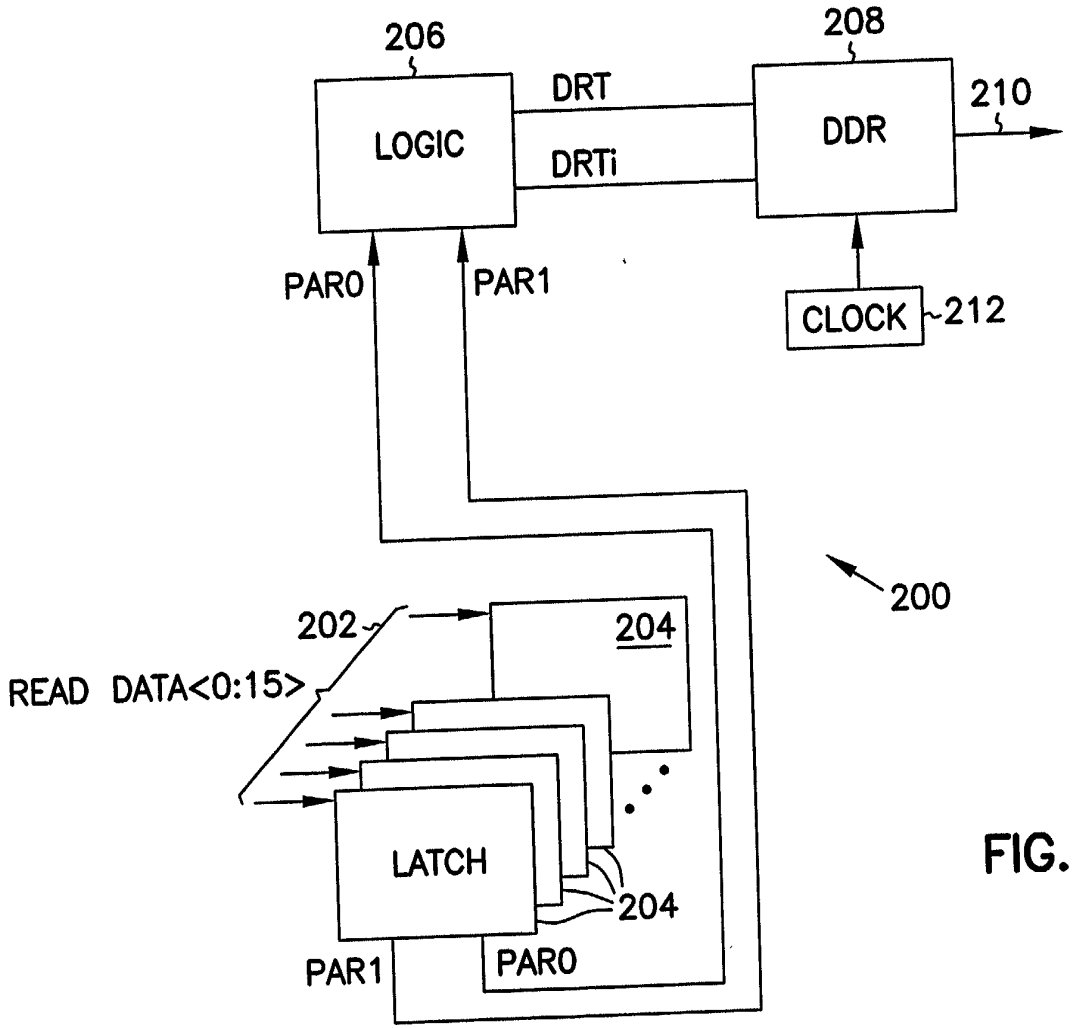
206
208
DRT
210
LOGIC
DDR
DRTi
PAR0
PAR1
CLOCK
212
200
202
204
READ DATA<0:15>
LATCH
204
PAR1
PAR0

FIG. 2

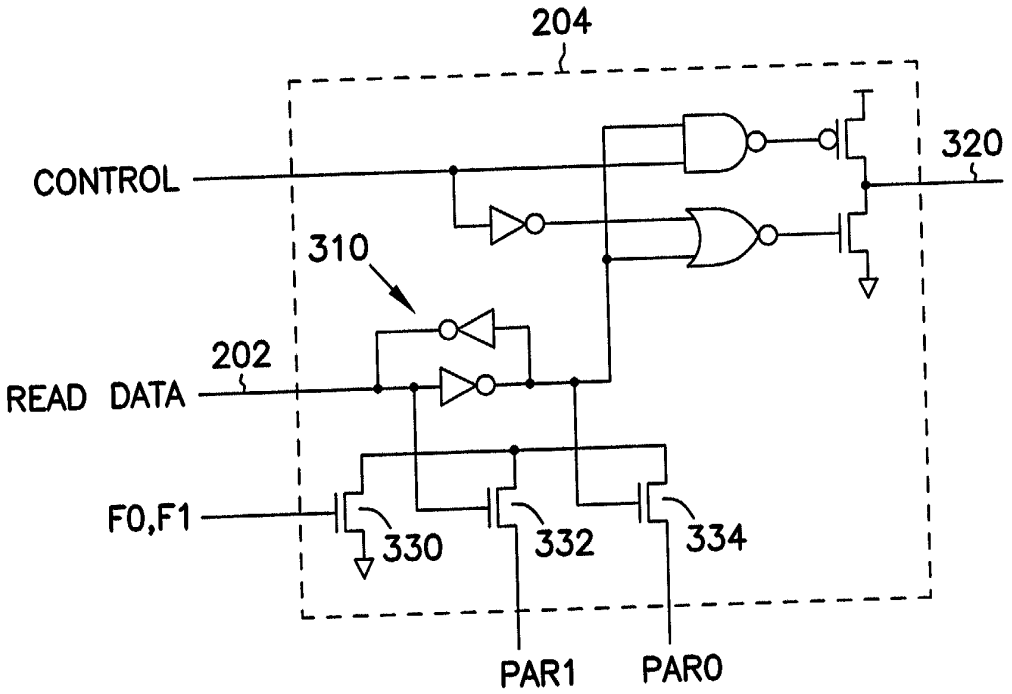

FIG. 3

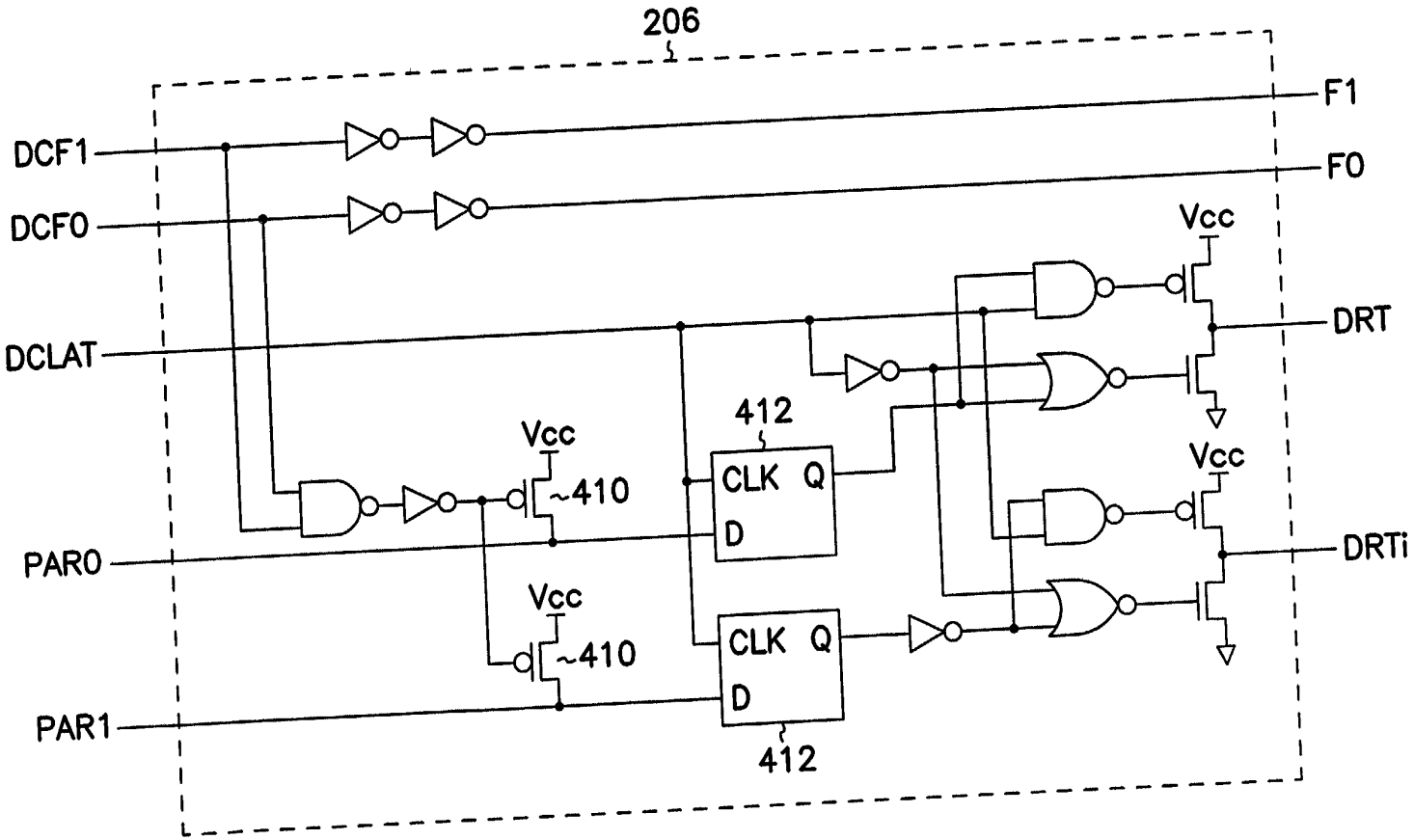

FIG. 4

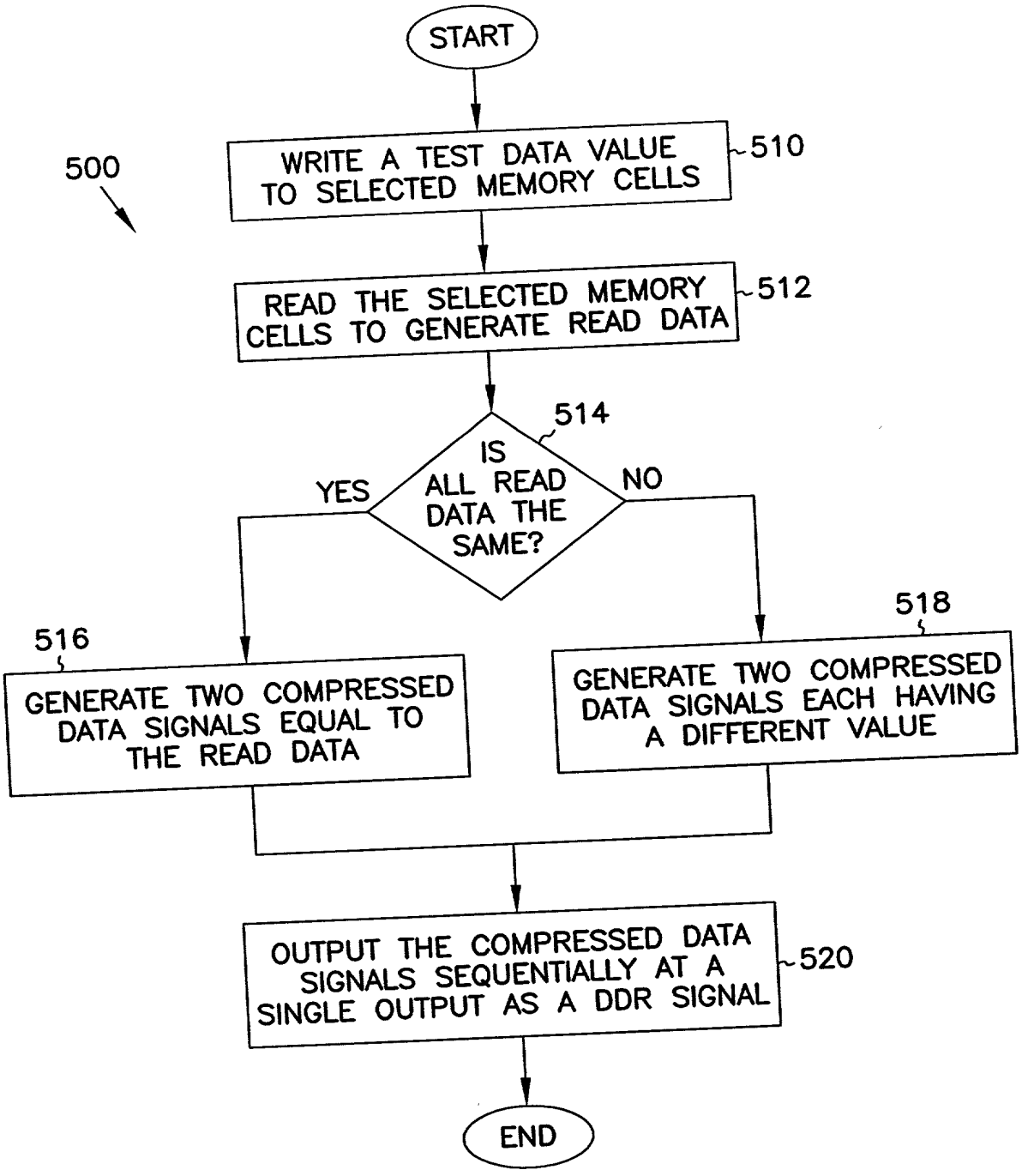
START
500
WRITE A TEST DATA VALUE TO SELECTED MEMORY CELLS
510
READ THE SELECTED MEMORY CELLS TO GENERATE READ DATA
512
514
IS ALL READ DATA THE SAME?
YES
NO
516
GENERATE TWO COMPRESSED DATA SIGNALS EQUAL TO THE READ DATA
518
GENERATE TWO COMPRESSED DATA SIGNALS EACH HAVING A DIFFERENT VALUE
OUTPUT THE COMPRESSED DATA SIGNALS SEQUENTIALLY AT A SINGLE OUTPUT AS A DDR SIGNAL
520
END

FIG. 5

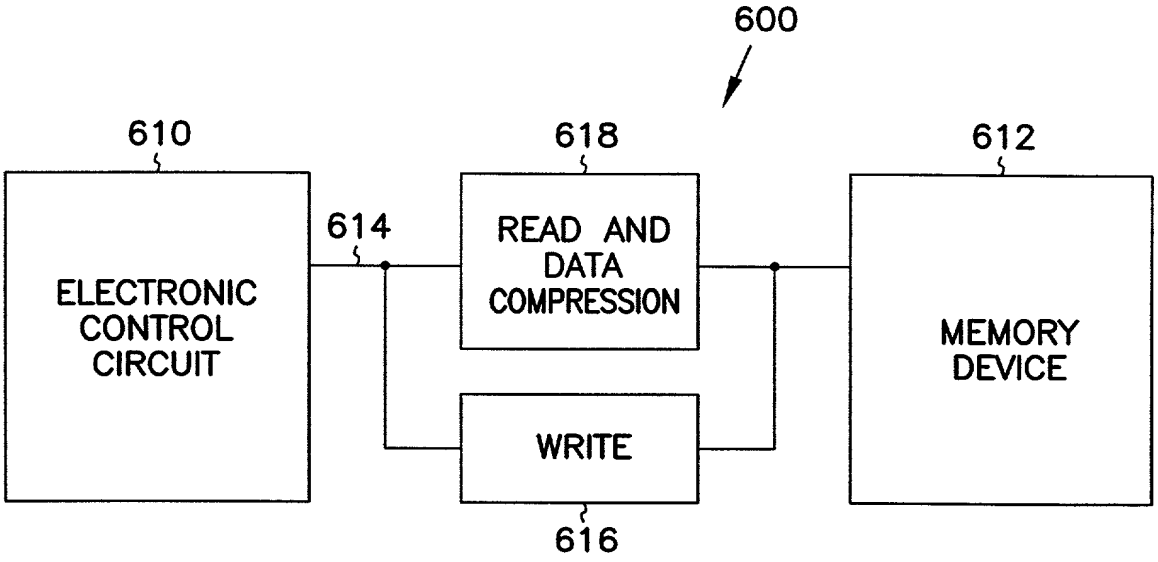
600
610
618
612
614
ELECTRONIC CONTROL CIRCUIT
READ AND DATA COMPRESSION
MEMORY DEVICE
WRITE
616

FIG. 6

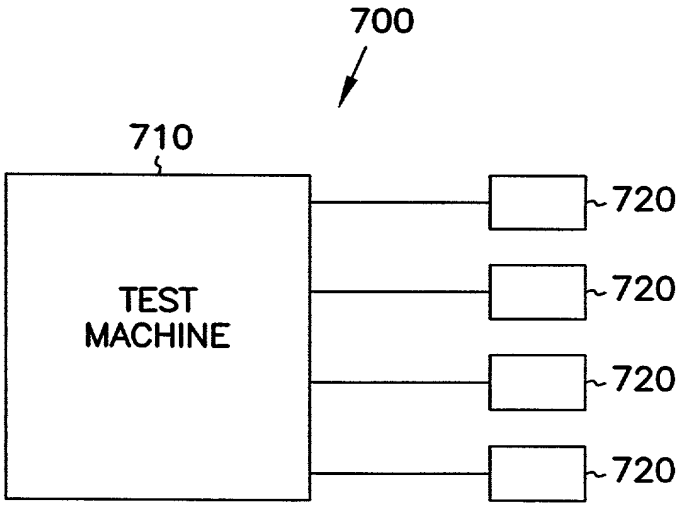
700
710
TEST MACHINE
720
720
720
720

FIG. 7

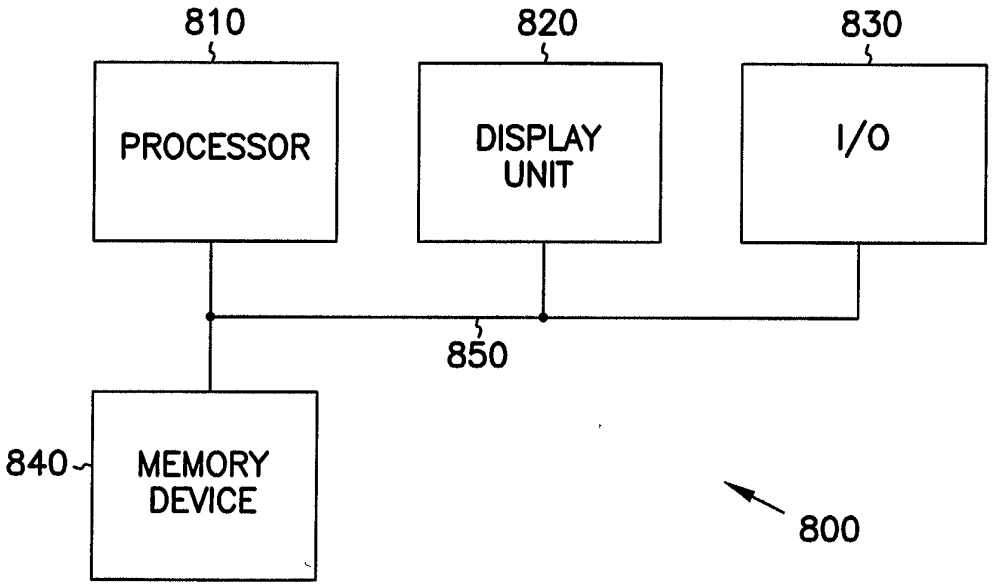
810
820
830
PROCESSOR
DISPLAY UNIT
I/O
850
840
MEMORY DEVICE
800

FIG. 8

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first an joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND APPARATUS FOR TESTING A MEMORY DEVICE WITH COMPRESSED DATA USING A SINGLE OUTPUT .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Signature: M. Mirmajid Seyyedy Date: 1-25-99
Mirmajid Seyyedy

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Post Office Address: 3608 Riva Ridge
Boise, ID 83709

Signature: Date: 1-26-99
Mark R. Thomann

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Mirmajid Seyyedy et al.	Examiner: Unknown	
Serial No.:	Unknown	Group Art Unit: Unknown	
Filed:	Herewith	Docket: 303.550US1	
Title:	METHOD AND APPARATUS FOR TESTING A MEMORY DEVICE WITH COMPRESSED DATA USING A SINGLE OUTPUT		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Adams, Matthew W.	Reg. No. P-43,459	Fogg, David N	Reg. No. 35,138	Lundberg, Steven W.	Reg. No. 30,568
Anglin, J. Michael	Reg. No. 24,916	Forrest, Bradley A.	Reg. No. 30,837	Mates, Robert E.	Reg. No. 35,271
Arora, Suneel	Reg No. 42,267	Harris, Robert J.	Reg. No. 37,346	McCrackin, Ann M.	Reg. No. 42,858
Bianchi, Timothy E.	Reg. No. 39,610	Holloway, Sheryl S.	Reg. No. 37,850	Padys, Danny J.	Reg. No. 35,635
Billion, Richard E.	Reg. No. 32,836	Huebsch, Joseph C.	Reg. No. 42,673	Polglaze, Daniel J.	Reg. No. 39,801
Black, David W.	Reg. No. 42,331	Kalis, Janal M.	Reg No. 37,650	Schwegman, Micheal L.	Reg. No. 25,816
Brennan, Thomas F.	Reg. No. 35,075	Klima-Silberg, Catherine I.	Reg. No. 40,052	Sieffert, Kent J.	Reg. No. 41,312
Brooks, Edward J., III	Reg. No. 40,925	Kluth, Daniel J.	Reg. No. 32,146	Slifer, Russell D.	Reg. No. 39,838
Clark, Barbara J.	Reg. No. 38,107	Lacy, Rodney L.	Reg. No. 41,136	Terry, Kathleen R.	Reg. No. 31,884
Drake, Eduardo E.	Reg. No. 40,594	Leffert, Thomas W.	Reg. No. 40,697	Viksnins, Ann S.	Reg. No. 37,748
Dryja, Michael A.	Reg. No. 39,662	Lemaire, Charles A.	Reg. No. 36,198	Woessner, Warren D.	Reg. No. 30,440
Embretson, Janet E.	Reg. No. 39,665	Litman, Mark A.	Reg. No. 26,390		

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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Dated: 1-28-99

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel